11) Publication number:

**0 396 248** Δ2

12

## **EUROPEAN PATENT APPLICATION**

21) Application number: 90303252.2

(51) Int. Cl.5: H01R 13/04

2 Date of filing: 27.03.90

® Priority: 17.04.89 JP 97009/89

② Date of publication of application: 07.11.90 Bulletin 90/45

Designated Contracting States:
DE FR GB

Applicant: AMP INCORPORATED 470 Friendship Road Harrisburg Pennsylvania 17105(US)

| 172 Inventor: Nakamura, Keiichi 6-8-14 Shimouma, Setagaya-ku Tokyo(JP) Inventor: Oshima, Tsutomu

Inventor: Oshima, Tsutomu 2-29-3 Chuo-cho, Meguro-Ku Tokyo(JP)

Inventor: Kitai, Toshihiko 1347-5 Higashi-Otake Isehara-shi, Kanagawa(JP) Inventor: Fukuda, Katsunori

2-12-23 Yaei

Sagamihara-shi, Kanagawa(JP)

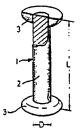
Representative: Warren, Keith Stanley et al BARON & WARREN 18 South End Kensington London W8 5BU(GB)

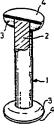
(54) Electrical pin and method for making same.

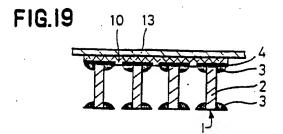
An electrical pin (1) comprises an electrically-conductive pin member (2) having the same diameter over its entire length and head members (3) secured at both ends of the pin member and having an enlarged surface greater in diameter than the pin member and in the same plane of the end surfaces of the pin member. A plurality of the pins (1) are maintained in alignment at a predetermined pitch by means of an electrically conductive layer (10) to which the head members (3) at one end of each pin member (1) is adhered and a dielectric member (13) to which the electrically conductive layer (10) is secured.

FIG.I

FIG.2







## **ELECTRICAL PIN AND METHOD FOR MAKING SAME**

5

10

20

35

This invention relates to an electrical pin and a method for making same. More specifically, the invention relates to a micro I/O pin and a method for making same for primarily interconnecting electrodes between a chip device such as a monolithic or hybrid IC (integrated circuit) and its packaging substrate.

1

Conventionally, it is typical to install a chip device such as a monolithic or hybrid IC onto a package substrate by mounting such chip device at a predetermined position on such package substrate and wirebonding between printed circuits on the substrate and the chip electrodes.

However, hybrid ICs are performing increased multiple functions, have higher packaging density and are more compact for rapidly-expanding applications for consumer electronic appliances. As a result, stronger needs arise for compact and less-expensive interconnections of such chip devices.

Conventional wirebonding means require bridging between electrodes of the package substrate and the chip device with fine gold or similar lead wires and subsequently welding at each junction point. Such chip packaging is slow and occupies a relatively large area on the precious chip substrate for such junction points, thereby making it more difficult to meet the aforementioned requirements. Additionally, such wirebonding limits signal propagation speed.

It has been proposed to directly weld electrodes of chip devices and package substrates in order to meet the requirements. This requires miniature electrical pins for interconnecting the electrodes therebetween.

It is, therefore, an object of this invention to provide miniature, less expensive and higher signal propagation speed electrical pins particularly suited for directly connecting chip devices and package substrates in these types of IC devices.

It is another object of this invention to provide a method of making such electrical pins without using photo etching.

For this end, the electrical pin according to the present invention comprises an electrically-conductive pin member and electrically conductive head members at both end surfaces of the pin member. The pin member has an essentially equal diameter over its entire length. The head members have enlarged surfaces flush with both end surfaces of the pin member.

At least one end surface of the enlarged end surfaces of the head members is coated with a film electrode material for protecting oxidation of such end surface.

It is preferable that a large number of such

pins, each comprising the electrically-conductive pin member with the head members, are supported at one end surface on a support plate.

Such construction simplifies the operation to directly mounting the pin members onto a carrier such as a chip device or a printed circuit board.

Embodiments of such electrical pins are described in detail hereunder. Each embodiment utilizes the following basic steps.

The electrical pin is easily made by arranging a large number of wires each comprising a metal core member acting as an electrically-conductive pin member and a plated layer of a different metal on the outer surface of the metal core member, forming a wire arranged assembly integrating such wires with hardened plastic before slicing such wire arranged assembly perpendicular to the arranged wires to obtain a processing member of a thickness substantially equal to the pin length, forming an electrically-conductive head member by plating integrally onto the pin member in recesses formed by etching the plated layer on the outer surfaces of the pin members on both upper and lower surfaces of the processing member, removably adhering a support plate on one end surface of the processing member, and sequentially removing the plastic between the arranged wires and the outer plated layer.

Embodiments of this invention will now be described by way of example with reference to the accompanying drawings, in which:

FIGS. 1 and 2 are perspective views partly in cross section of different embodiments of the electrical pins according to the present invention.

FIGS. 3 through 19 illustrate the steps of making the electrical-pins according to the present invention.

FIGS. 20 through 22 illustrate the steps of installing the electrical pins of the present invention onto a substrate.

FIGS. 23 through 30 illustrate the steps of forming electrical junction points on a package substrate.

Illustrated in FIGS. 1 and 2 are two embodiments of the electrical pin according to the present invention. The pin 1 in FIG. 1 comprises an electrically-conductive pin member 2 and electrically-conductive head members 3 at both ends of the pin member, the head members 3 being of larger diameter than the pin member. The pin 1 in FIG. 2 has an electrically-conductive film 4 on the outer surface of the head members 3 acting as an oxidation protection film. The pin member 2 is made of an electrically-conductive metal such as copper or its alloy. Its length L and diameter D are,

20

30

45

50

for example, about 0.6-0.9 mm and 0.1 mm, respectively. The diameter includes a circumferential gold-plated layer of 0.1 m in thickness. The head members 3 are an electrically-conductive layer such as, for example, copper that is integrally formed on the circumferential surface of the edge portions of the pin member 2. The electrically-conductive film 4 is made of an alloy, for example, gold and tin. The transverse cross sections of the pin member 2 and the head members 3 are preferably circular but may be any other shape.

Although not shown in FIGS. 1 and 2, either one of the end surfaces of the electrically-conductive pin member 2 may be constructed in one of the above modes and the other end surface in the other mode in a further embodiment.

Illustrated in FIGS. 3 through 30 are basic steps common to the above modes of making the electrical pin.

Shown in FIG. 3 is a metal wire 5 to be the aforementioned electrically-conductive pin member 2. The wire 5 is an elongated wire of the above pin member 2 plated with a 0.1 mm thick layer 6 of tin or iron.

A plurality of such wires 5 are disposed between both ends of a holder (not shown) at a predetermined pitch (equal to the pitch of electrodes on a wiring board). Then, the holder is filled with a conventional dielectric material 7 such as a resin and the resin is hardened as an elongated member 8 as shown in FIG. 4.

The hardened member 8 is sliced at a predetermined length L of the pin members 2 perpendicular to the length of the arranged wires 5 as shown in FIG. 5, thereby providing processing members 9. Illustrated in FIG. 6 is one of such sliced processing members 9 which comprises a predetermined number of pin members 2 having both ends extending to upper and lower surfaces of the member 9 while being buried therein. A part of the cross section of the processing member 9 is illustrated in a magnified form in FIG. 7. In this condition, both upper and lower surfaces of the processing member 9 are polished to normalize the thickness and to smooth the surfaces.

The processing member 9 is then transported to subsequent processing steps as illustrated in FIGS. 8-19.

In the step of FIG. 8, an electrically-conductive layer 10 is formed by coating or depositing silver paste on the bottom surface of the processing member 9.

In the step of FIG. 9, the processing member 9 is dipped in an etching liquid for etching the plated layer 6 at the exposed surface of the processing member 9. As time elapses, dish-like recesses 11 around the pin members 2 are formed in the exposed surface, the recesses 11 being relatively

deep at the periphery of each pin member 2 due to its electrical conductivity but relatively shallow at the non-electrical conductive resin 7.

Subsequently, in FIG. 10, electrical current is supplied to the electrically-conductive layer 10 as a common electrode while dipping the processing member 9 in a plating bath. Copper-plated members 12 are formed onto the ends of the pin members 2 exposed in the recesses 11. The copper-plated members 12 are polished along the surface of the processing member 9 to obtain the electrically-conductive head members 3 with smooth outer surfaces as illustrated in FIG. 11.

In FIG. 12, a gold-plated, electrically-conductive film 4 is formed on the polished surfaces of the head members 3 as an electrode material for oxidation protection purposes. This step is adopted to protect oxidation of the end surfaces of the pin members 2 and the head members 3 during delivery or storage before actual use of the pins 1.

It is, therefore, understood that the last mentioned step may be eliminated in the event that the pins are used immediately after making, thereby avoiding oxidation of the end surfaces.

Illustrated in FIGS. 13 through 17 are the steps of providing similar head members 3 on the other surface of the processing member 9 to form the head members on the ends of the pin members 2 at the other surface.

Such additional steps are as follows: In FIG. 13, the electrically-conductive layer 10 acting as the common electrode for electro-plating is removed by conventional practices from the processing member 9 and the electrically-conductive layer 10 is formed on the other surface. Additionally, a ceramic plate 13 is adhered to the layer 10 for maintaining the alignment of the pin members 2 during subsequent processing and installation on a substrate.

Consequently, recesses 11 are formed in the other surface by fetching (FIG. 15), copper-plated portions 12 are formed in the recesses 11 and on the peripheries of pin members 2 (FIG. 16) and finally the head members 3 are completed on the other surface of the processing member 9 as shown in FIG. 17.

A gold-plated, electrically-conductive film 4 is provided on the end surfaces of the newly-formed head members 3 at this stage in order to obtain the particular pin 1 as illustrated in FIG. 2.

In FIG. 18, the resin between the arranged metal wires 5 in the processing member 9 is dissolved using an appropriate organic solution such as an aromatic or hydrocarbon solution. Although space is created between adjacent metal wires 5 by removing the resin, the metal wires 5 remain in their positions because of the ceramic plate 13.

FIG. 19 shows a finishing step to fill a dissolv-

ing liquid in the space of the resin for completely dissolving the plated layer 6 on the outer surface of the pin members 2. As a result, the arranged pins 1 without the plated layers 6 remain on the ceramic plate 13.

The pins 1 may be coated with the electricallyconductive film 4 on one end surface as shown in this embodiment, or coated with film 4 on both end surfaces. Alternatively, such film may be completely omitted.

The pins 1 are ready for installation steps as illustrated in FIGS. 20 through 22. A solder layer 22 is preformed on each junction point 21 on a printed circuit board of an IC chip ceramic substrate 20. The junction points 21 having the solder layer 22 are aligned with the particular arrangement of the pins 1 supported on the ceramic plate 13. The pins 1 and the junction points 21 on the ceramic substrate 20 are aligned (as shown in FIG. 20) in such a manner that each pin 1 is pressed on the solder layer 22 at each junction point 21. The solder layers 22 are heated, thereby making solder electrical connections of the pins 1 to respective junction points 21 as shown in FIG. 21.

In a final step as shown in FIG. 22, the ceramic plate 13 supporting the pins is removed along with the electrically-conductive layer 10.

Consequently, the pins 1 are firmly mounted and electrically connected to the respective junction points 21 on the ceramic substrate 20 at their bottom ends while the upper ends are ready to receive electrodes of an IC chip device.

Illustrated in FIGS. 23 through 30 are steps to form the aforementioned ceramic substrate 20. The ceramic substrate 20 acting as an electrical-shielding plate and an electrode plate has printed circuits and the junction points 21 preformed on the surface (see FIG. 23). A photoresist layer 23 is applied on the surface (FIG. 24) covering such surface and the junction points 21.

In FIG. 25, the junction points 21 are covered with sections of a mask 24 to prevent exposure of light from a light source 25 whereas the photoresist layer 23 is exposed to light through openings of the mask 24. This will harden exposed regions 23a of the photoresist layer 23.

In the step of FIG. 26, the non-hardened regions of the photoresist layer 23 covering junction points 21 are conventionally removed by washing, etching or scribing of the photoresist layer 23. This leaves the hardened exposed regions 23a of the photoresist layer 23 surrounding the junction points 21

In FIG. 27, the junction points 21 are covered with either a silver or tin layer 26 by a conventional plating technique.

Also, in FIG. 28, a layer 27 of the complementary metal (either tin or silver) is formed on the

layer 26.

In FIG. 29, the hardened regions 23a are removed by washing, etching or scribing means. Subsequently, in FIG. 30, heat processing is performed of the two layers 26 and 27 to form an alloy of the two metals acting as the above solder layer 22

According to the electrical pin of the present invention, a chip device such as monolithic or hybrid ICs can be directly connected to a package substrate. The pin is so small that it is very effective to miniaturize connections of such IC devices, to reduce production cost, and to increase signal propagation speed.

The head member of the electrical pin is enlarged in diameter by the plated electrically-conductive material on the circumference of the pin member at one or both ends, thereby increasing the mounting strength as compared with the pin without such head member.

The formation of the electrode film material on the end surface of the head member helps to prevent such surface from oxidation during storage, delivery or when it is actually installed, thereby avoiding any problems such as degraded electric connection or generated heat due to increased resistance at the junction points.

Also, a large number of electrical pins are supported in an up-right position on a support plate in such a fashion to coincide with the electrodes of the chip device, printed circuit board or carrier member to be interconnected thereby. In this way, the arrangement of the pins is maintained and the support plate is subsequently removed, thereby allowing the pins to be soldered automatically at the head members on a carrier member.

The method of making the electrical pins according to the present invention allows the easy and simultaneous making of a large number of electrical pins having head members at both end surfaces.

All etching processing are conventional and well established. Additionally, two or more different photoetching technologies are not required to be used, thereby making the processing relatively simple, and the product quality very high and easily controllable.

## Claims

1. An assembly of electrical pins, each electrical pin comprising an electrically-conductive pin member (2) and electrically-conductive head members (3) at both ends of said pin member wherein said pin member is substantially the same diameter over the entire length and said head members have an enlarged surface greater in diameter than

20

30

35

40

45

50

said pin member, and means (10, 13) maintaining a plurality of said electrical pins in alignment at a predetermined pitch, characterized in that said means comprising an electrically-conductive layer (10) to which the head members (3) at one end of said pin members (2) are adhered, and a dielectric member (13) to which said electrically-conductive layer (10) is secured.

- 2. An assembly of electrical pins as claimed in claim 1, characterized in that the end surfaces of said head members (3) are in the same plane of the end surfaces of said pin member (2).
- 3. An assembly of electrical pins as claimed in claim 2, characterized in that an electrically-conductive film (4) is disposed between said head members (3) at the one end of said pin members (2) and said electrically-conductive layer (10).
- 4. An electrical pin comprising an electrically-conductive pin member (2) and electrically-conductive head members (3) formed at both ends of said pin member, characterized in that said pin member is substantially the same diameter over the entire length and said head members (3) have an enlarged surface greater in diameter than said pin member (2) and in the same plane of the end surfaces of said pin member.
- 5. An electrical pin as claimed in claim 4, characterized in that at least one of said enlarged end surfaces of said head members (3) has an electrically-conductive film (4) secured thereover.
- 6. A method of making electrical pins, characterized by the steps of arranging a large number of wire members (5) having metal pin members (2) coated with a layer (6) of different metal in alignment at a predetermined pitch;

applying a dielectric material (7) to the arrangement of wire members (5) which upon hardening forms an elongated member (8);

slicing the elongated member (8) perpendicular to the wire members (5) to obtain a processing member (9) having a thickness equal to the length of the electrical pins;

removing said metal layers (6) of said wire members (5) at both ends of said pin members (2) thereby forming recesses (11) around both ends of the pin members (2);

plating a conductive metal (3) in said recesses (11) forming head members (3) secured to the ends of the pin members (2);

securing an electrically-conductive layer (10) to the head members (3) at one end of the pin members (2); and

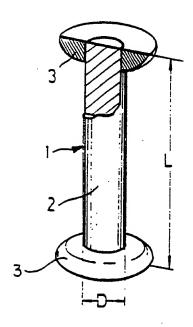
removing the dielectric material (7) and the metal layers (6).

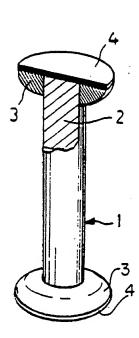
7. A method of making electrical pins as claimed in claim 6, characterized by the further step of forming a film electrode (4) on the head

members (3) at one end of the pin members (2).

FIG.I







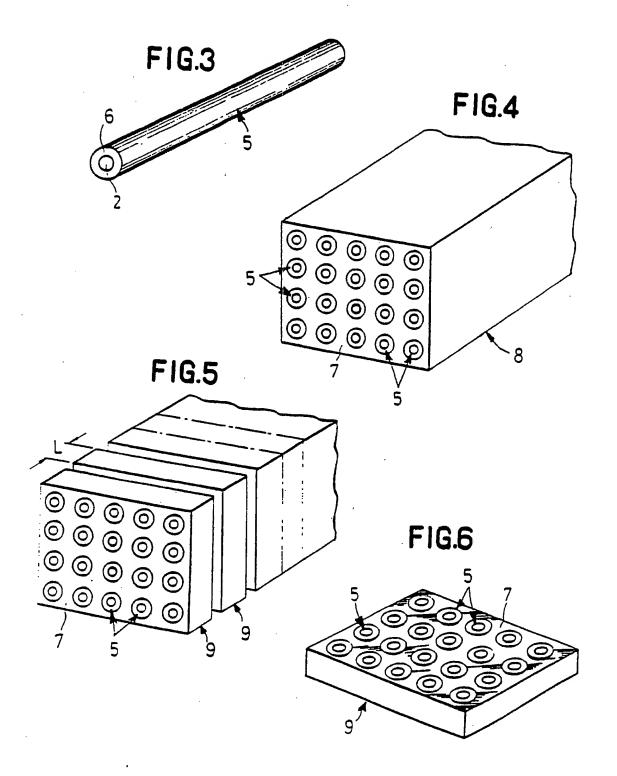


FIG.7

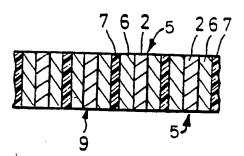


FIG.10

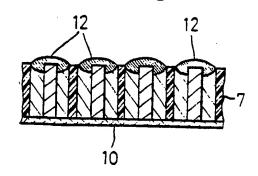


FIG.8

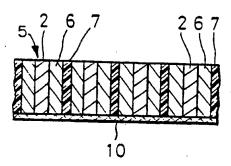


FIG.11

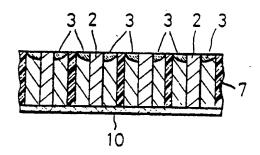


FIG.9

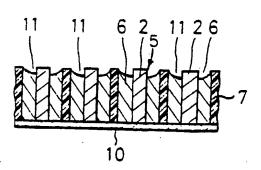


FIG.12

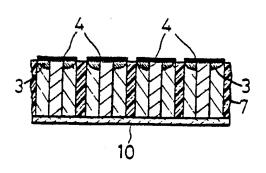


FIG.13

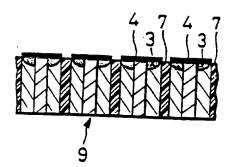


FIG.16

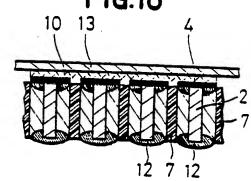


FIG.14

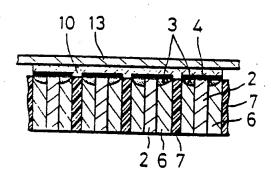


FIG.17

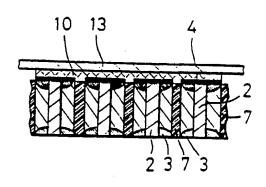


FIG.15

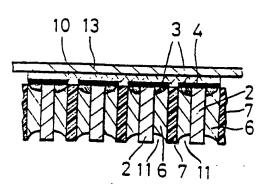
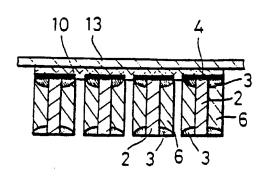
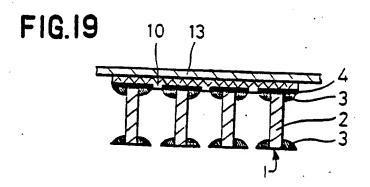
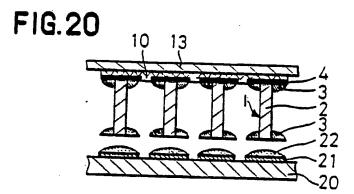


FIG.18







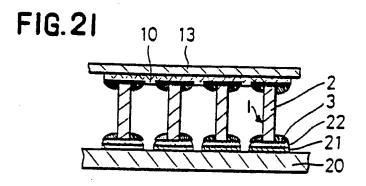


FIG.22

